AREA EFFICIENT DECIMATION FILTER BASED ON MERGED DELAY TRANSFORMATION FOR WIRELESS APPLICATIONS

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Expected by 2014 is the 4G standard for cellular wireless communications, which will improve bandwidth, connectivity and roaming for mobile and stationary devices.4G and other wireless systems are currently hot topics of research and development in the communication field. In wireless technologies like Global System for Mobile (GSM), Digital Enhanced Cordless Telecommunications (DECT) and Wi-Fi, decimation filters are essential part of transceivers being used. This paper describes a decimation filter which is efficient in terms of both the power consumption and the area used. The architecture is based upon Merged Delay Transformation (MDT). The existing Merged Delay Transformed Infinite Impulse Response (IIR) architecture is power efficient but requires larger area. The proposed and existing filters were implemented on Field-Programmable Gate Array (FPGA). The computational cost of the proposed filter is reduced to (3N/2 + 1) and M-1 times reduction in the number of multipliers in comparison to the existing FIR filter is achieved. The power consumption and speed remain nearly the same.

Keywords: Area efficient architecture, Decimation filter, Merged delay transformation, Recursive filter

1. Introduction

Wireless solutions are needed in a wide range of consumer electronic applications. Most of these applications use wireless technologies like GSM, DECT and Wi-Fi and decimation filters are an essential part of transceivers being used for these standards [2-5]. Therefore there is always an increasing demand for power, area and speed efficient architectures of decimation filter [1, 3].

The recent approach in this direction is to use Cascaded Integrator Comb (CIC) filter with a Finite Impulse Response (FIR) filter to meet the design requirements [1-3]. The major advantages of this approach are the multiplier less CIC comb filter with a cascaded linear phase FIR filter. However, the increased complexity of FIR filters to meet design specification increases area and power consumption [6]. Also the higher order FIR filters have larger critical path delay which requires faster hardware for implementation.

Compared to FIR filters IIR filters need lesser hardware and improved critical path delay [7]. For [8, 9] improving the efficiency of IIR filter an architecture based on Merged Delay Transformation has been proposed [8, 9]. This new architecture has the advantage of being efficient in terms of power consumption as it runs at lower output frequency [9]. But it requires large hardware for its implementation.

In this paper we have proposed a modification to existing MDT recursive decimator so that its demand for larger silicon area is considerably reduced while keeping its power consumption almost at the same level.

The next section briefly describes the Merged Delay Transformation alongwith Decimator based on this transformation. In section 3 the detailed discussion of the modification to existing architecture is provided. Section 4 discusses implementation of decimation filters and carries out the comparison between existing decimation filters and the proposed architecture. Section 5 concludes the paper.

2. Merged Delay Transformed Recursive Decimation Filter

2.1. Merged Delay Transformation

Merged Delay Transformation (MDT) is applied on first order recursive filter so that output is obtained for M^{th} previous sample. This Transformation is explained in [8, 9].The output of first order recursive filter is given as

$$y[n] = py[n-1] + rx[n] \qquad (1)$$

Applying MDT it can be written as

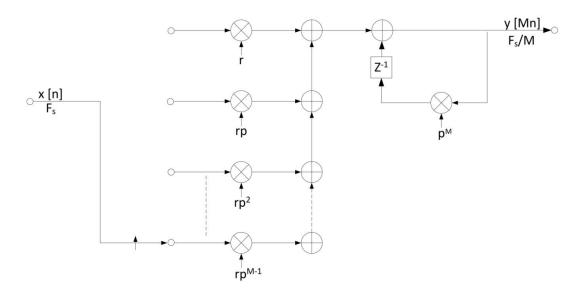$$y[n] = p^M y[n-M] + \sum_{k=0}^{M-1} p^k r x[n-k] \qquad (2)$$

Figure 1.   Decimator filter obtained by MDT on first order recursive filter [5].

This equation can be implemented employing one feedback path and M feed forward paths [8]. For a recursive filter of order N, p and r are generally complex. This fact leads to an implementation employing complex multiplications. This complexity can be simplified by pairing up two first order sections to obtain a second order section with real p and r.

The equation for second order recursive filter obtained from two single order sections is given as

$$y_{out} = y_1[n] + y_2[n] \qquad (3)$$

As first order sections have pole and zero which are complex conjugate of each other so

$$y_{1R}[n] = y_{2R}[n] \qquad (4)$$

and

$$y_{1I}[n] = -y_{2I}[n] \qquad (5)$$

So (3) becomes

$$y_{out} = 2y_{1R}[n] \qquad (6)$$

Applying MDT transformation on (6) as explained in [8] the transfer function for second order section can be written as given below.

$$y_{out}[z] = 2\frac{\sum_{k=0}^{M-1} H_k(z^M)z^{-k}}{1 - A_F z^{-M} - B_F z^{-2M}} \qquad (7)$$

This equation leads to parallel implementation of Merged Delay Transformed Recursive filter

using second order sections with only real multiplications.

2.2.   MDT Based Recursive Decimator

Using equations (2), (7) and employing Nobel identities [9] of digital signal processing architecture for decimation filters can be obtained as explained [9] and shown in Figures 1 and 2 respectively.

The Sub-filter $H_k(z)$ is unfolded and shown in Figure 3. Coefficients for each sub-filter can be obtained by equations [8].

The major advantage of this architecture is that all components of recursive decimator work at low output frequency which decreases its power consumption [9]. However, it is quite evident that to compute each output sample we require M + 1 multipliers for each first order section, increasing the silicon area required for this implementation. In next section we propose an area efficient implementation of this structure.

3.   Area Efficient MDT Decimator

The MDT Decimation filter shown in Figure 1 and Figure 2 operate at low frequency of the input clock a desired factor in multi-rate filters. But 'M' parallel sections in the filter require (M+1) multipliers significantly increasing the cost and power consumption of the MDT decimation filter. As the decimation Factor 'M' becomes larger the cost and power increases proportionally leaving the filter implementation impracticable.
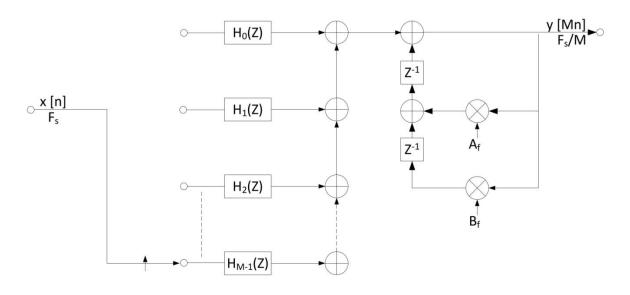
Figure 2.   Decimator filter obtained by MDT on second order recursive filter [5].
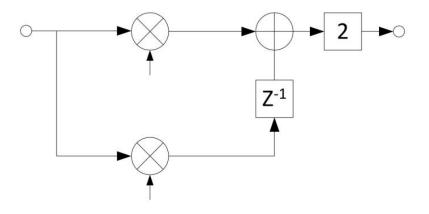

Figure 3.   Sub filter $H_k(z)$ Unfolded with coefficients from [4].

An area efficient implementation for first order section can be achieved for MDT decimator by replacing the M multipliers in feed forward paths with a single multiplier and M sample accumulator. The coefficients are being multiplexed at high input frequency.

The multiplier and accumulator both are working at high input frequency however the accumulator updates its output after M samples so remaining structure is working at low output frequency as shown in Figure 4.

A similar implementation can be achieved for second order section as shown in Figure 5. The coefficients for second order section are derived and explained [8, 9].

This implementation requires 2 multipliers per first order section decreasing the area demand for implementation however one of the multipliers is working at higher input frequency increasing its power consumption.

4.   Implementation and Results

In first part, the proposed filter and MDT are modeled in Simulink for functional verification and detail filter comparison is provided. The second part gives the detail discussion on simulation and implementation of several existing filters with the proposed filter for GSM application. The last part provides the filter response and discusses the stability of the proposed filter.
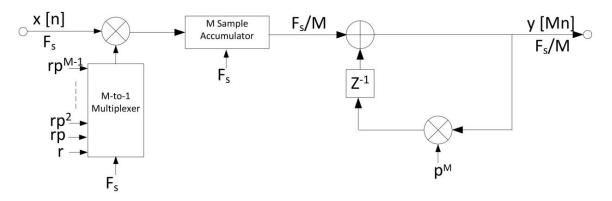
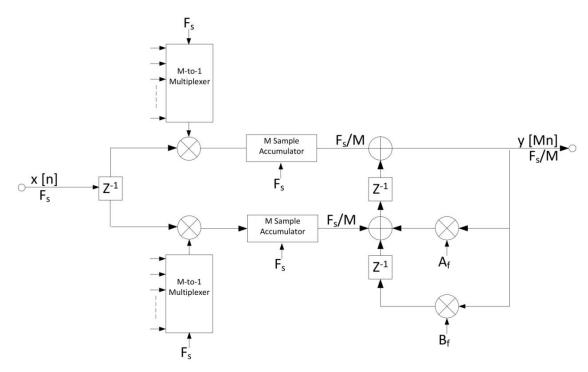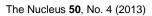Figure 4.   Modified MDT Decimation filter obtained from first order recursive filter.

Figure 5. Modified MDT decimation filter obtained from second order recursive filter.

4.1.   *Functional Verification and Comparison*

Figure 6 shows the block diagram of the MDT and proposed Modified MDT filter modeled in Simulink for functional verification where both the filters are implemented using 2nd order sections. The internal structure of MDT filter is shown in Figure 7 having down-samplers to implement commutator architecture requiring (M-1) multipliers. The Structure of the proposed filter in Figure 8 employs switch to select from the coefficients having a single multiplier. The outputs of filters are shown in Figure 9 and the error is zero. The error in comparison to IIR and FIR filters are plotted in Figure 10.

For 'N' filter order and decimation factor 'M' the costs in terms of multiplication of FIR filter is MN, while IIR filter has (2N + 1)M multipliers and MDT requires (N + NM/2) multiplications per sample output [8].The proposed filter reduces the complexity of the MDT filter by replacing the multipliers in parallel 'M' sections into a single multiplier by multiplexing the coefficients. The overall computation cost in terms of multiplication of the proposed filter is reduced to (3N/2 + 1) therefore reducing the computational cost by a factor (M-1)/2 compared with MDT and almost a factor of M-1 in comparison to FIR filter.
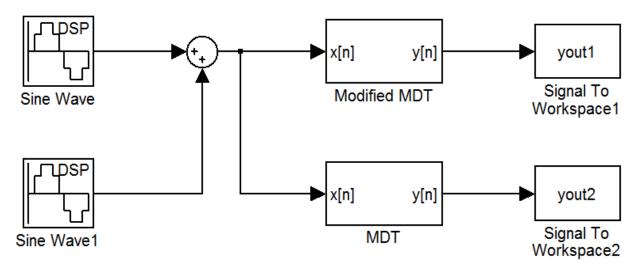
Figure 6. Modified MDT and MDT decimation filter comparison architecture.
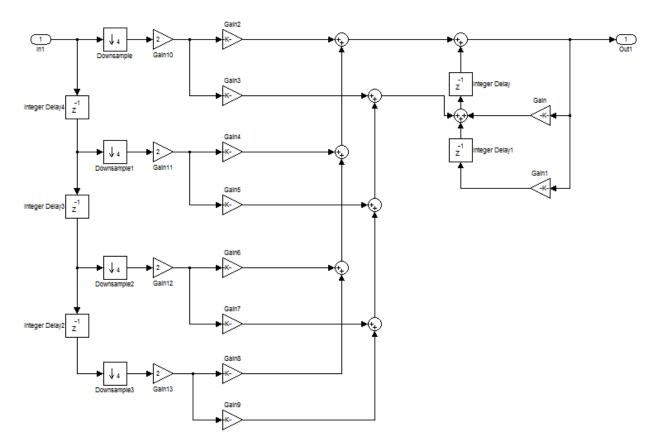

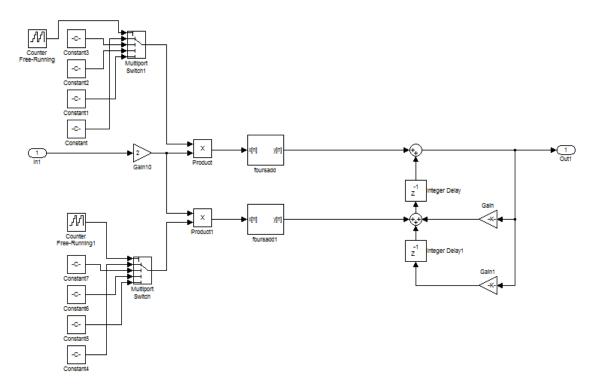Figure 7. MDT decimation filter internal structure.

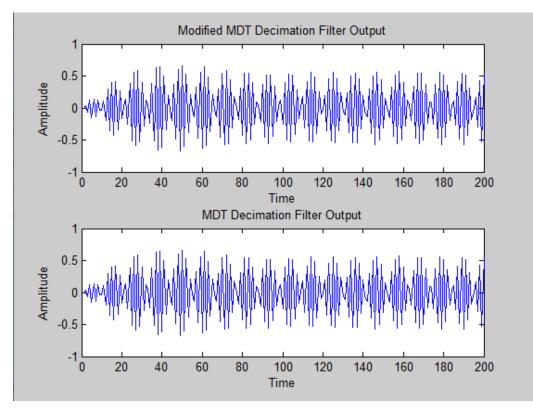Figure 8.   Modified MDT decimation filter internal structure.

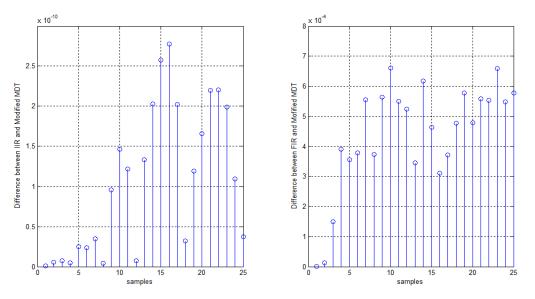Figure 9.   Modified MDT and MDT decimation filter outputs.

Figure 10.   The difference between outputs of IIR vs. modified MDT and FIR vs. modified MDT filters.

4.2.   Filter Simulation and Implementation for GSM Application

4.2.1.   Filter Specifications

In order to compare different filter architectures suitable for application under consideration FIR, IIR, MDT and Modified MDT decimator were designed with the following specifications [1]: input sampling frequency 1.0833 MHz, pass band ripple less than 0.1dB, stop band attenuation greater than 96dB and decimation factor M=4. An IIR Filter of order 12 and FIR filter of order 251 meets these specifications.   MDT and Modified MDT were converted from IIR filter coefficients with same order.
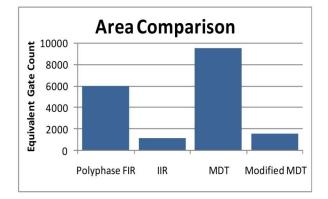

Figure 11. Hardware area comparison of different architectures in terms of equivalent gate count.

4.2.2.   Filter Implementation

IIR filter was implemented as cascade of second order sections. Efficient polyphase implementation of FIR filter was achieved by replacing M sub filters with single filter and its coefficients being multiplexed at high input frequency [11]. All these architectures were converted to fixed point form [10] and then implemented on FPGA.

The Verilog codes for all the above mentioned decimation filters were synthesized. For silicon chip area Equivalent Gate Count was used as metric to compare these filters as shown in Figure 11.

Power consumption of above mentioned architectures was practically measured and the comparison is given in Figure 12.
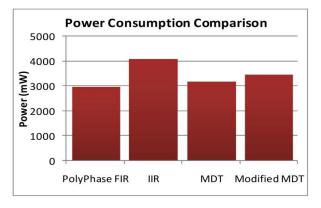

Figure 12. Power consumption of four architectures in mW.

As it is clear from Figure 11, the area requirement for Modified MDT decimation filter is considerably less than MDT decimator as well as FIR decimator. On the other hand power

consumption of Modified MDT is higher than MDT decimation filter however it is comparable to FIR decimator. An improvement in the combinational delay is also observed where MDT has 35 ns delay and Modified MDT has 28 ns delay.

4.2.3. Filter Response and Stability

An IIR filter with the given specification is designed in Matlab. The entire poles lie inside of unit circle hence the IIR filter is stable as shown in Figure 13. The IIR filter is first transformed using MDT and then into the proposed architecture. The pole zero plots obtained for IIR filter and Proposed MDT are shown in Figure 12. The poles lie inside the unit circle for proposed filter and the transformation results in stable filter. The Magnitude and Phase responses are shown in Figure 14.
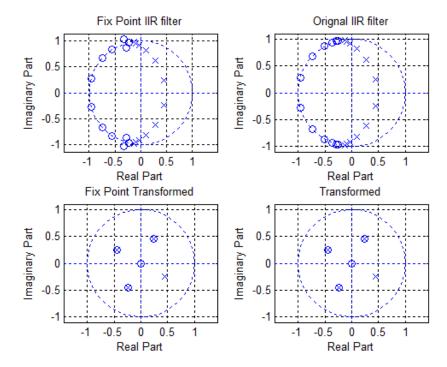

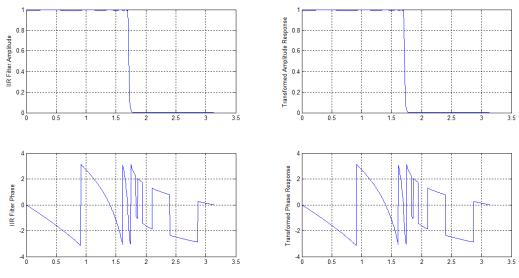Figure 13. Pole zero plot of IIR Decimation filter and Modified MDT Decimation filter.

Figure 14. Magnitude and Phase responses of IIR and Modified MDT Decimation filters.

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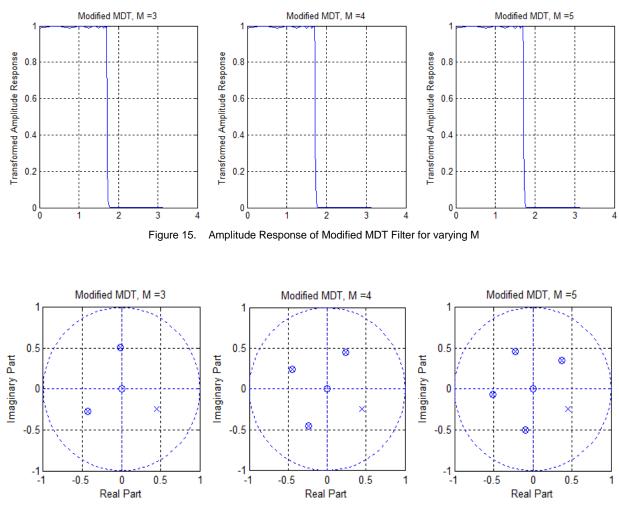Figure 15.   Amplitude Response of Modified MDT Filter for varying M

Figure 16.   Pole zero plot for Modified MDT Filter for varying M.

The proposed architecture efficiently introduces (M-1) poles within the unit circle. Equal number of zeros is also introduced at the location of poles to maintain the Magnitude response. It is observed that by changing the factor M does not change the magnitude response of the filter and stability is not affected as shown in Figures 15 and 16 respectively.

5.   Conclusion

The Modified MDT decimation filter proposed in this paper has an advantage of about 70% lower silicon area requirement for the application considered over existing MDT decimation filters. The computational efficiency improves to (3N/2) which is highly suitable for wireless applications where high order filter is required.

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